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APPLICATION

FOR

UNITED STATES LETTERS PATENT

APPLICANT NAME: **Douglas D. Coolbaugh, Peter B. Gray, Donna K. Johnson, Michael J. Zierak**

TITLE: **Passivation for Improved Bipolar Yield**

DOCKET NO.: **BUR920000143US1**

INTERNATIONAL BUSINESS MACHINES CORPORATION

PASSIVATION FOR IMPROVED BIPOLAR YIELD

DESCRIPTION

Field of the Invention

The present invention relates to heterojunction bipolar transistors, and more particularly to a method of fabricating a SiGe heterojunction bipolar transistor in which the SiGe bipolar yield is improved by protecting the edges, i.e., sidewalls, of the bipolar emitter with a passivation layer prior to siliciding the silicon surfaces of the bipolar transistor.

Background of the Invention

Significant growth in both high-frequency wired and wireless markets has introduced new opportunities where compound semiconductors such as SiGe have unique advantages over bulk complementary metal oxide semiconductor (CMOS) technology. With the rapid advancement of epitaxial-layer pseudomorphic SiGe deposition processes, epitaxial-base SiGe heterojunction bipolar transistors have been integrated with mainstream advanced CMOS development for wide market acceptance, providing the advantages of SiGe technology for analog and RF circuitry while maintaining the full utilization of the advanced CMOS technology base for digital logic circuitry.

A typical prior art SiGe heterojunction bipolar transistor is shown, for example, in FIG 1. Specifically, the SiGe heterojunction bipolar transistor shown in FIG 1 comprises semiconductor substrate 10 of a first conductivity type having sub-collector 14 and collector 16 formed therein. Isolation regions 12, which are also present in the substrate, define the outer boundaries of the bipolar transistor. The bipolar transistor of FIG 1 further includes SiGe layer 20 formed on a surface of substrate 10 as well as isolation regions 12. The SiGe layer includes polycrystalline Si regions 24 that are formed over the isolation regions and SiGe base region 22 that is formed over the collector and subcollector regions. The prior art bipolar transistor also includes patterned insulator layer 26 formed on the base region and emitter 28 formed on the patterned insulator layer as well as a surface of SiGe base region 22. Silicide regions 30 are also present in the structure shown in FIG 1.

A major problem with the prior art SiGe heterojunction bipolar transistors of the type illustrated in FIG 1 is that the SiGe bipolar yield is significantly reduced because of the presence of shorts which are introduced into the structure during the silicide process. The shorts are caused by the presence of silicide bridges that exist in the structure. As such, a 20-30% yield loss is typically associated with prior art SiGe heterojunction bipolar transistors. The SiGe bipolar yield loss is more pronounced when cobalt disilicide regions are formed in the structure.

In view of the above mentioned problem with prior art heterojunction bipolar transistors, there is still a continued need for developing a new and improved method which is capable of fabricating a heterojunction bipolar transistor in which the SiGe bipolar yield loss due to silicide shorts has been substantially eliminated.

Summary of the Invention

One object of the present invention is to provide a method of fabricating a SiGe heterojunction bipolar transistor wherein improved SiGe bipolar yield is achieved.

Another object of the present invention is to provide a method of fabricating a SiGe heterojunction bipolar transistor wherein the shorts caused during the formation of silicide regions in the structure are substantially eliminated.

A further object of the present invention is to provide a method of fabricating a SiGe heterojunction bipolar transistor which prevents bridging between adjacent silicide regions.

An even further object of the present invention is to provide a method of fabricating a SiGe heterojunction bipolar transistor using processing steps that are compatible with existing bipolar and CMOS (complementary metal oxide semiconductor) processing steps.

These and other objects and advantages are achieved in the present invention by protecting the edges of the emitter with a passivation layer prior to the formation of silicide regions in the structure. The passivation layer is formed on the edges of the emitter in the present invention by utilizing a rapid thermal chemical vapor deposition

(RTCVD) process which is capable of providing a conformal layer thereon. The passivation layer employed in the present invention may be composed of a nitride, an oxide, an oxynitride or any combination thereof.

Specifically, the method of the present invention comprises the steps of:

(a) forming a passivation layer on at least exposed sidewalls of an emitter, said emitter is in contact with an underlying SiGe base region through an emitter opening formed in an insulator layer; and

(b) siliciding any exposed silicon surfaces so as to form silicide regions therein.

In accordance with the present invention, the passivation layer is formed from a rapid thermal chemical vapor deposition process which is capable of forming a conformal layer of passivating material on the sidewalls of the emitter. The passivating layer employed in the present invention may be composed of a nitride, an oxide, an oxynitride or any combination thereof. Of these passivating materials, it is highly preferred in the present invention that the passivation layer be composed of a nitride.

Another aspect of the present invention relates to the SiGe heterojunction bipolar transistor that is fabricated from the above-mentioned processing steps. Specifically, the inventive SiGe heterojunction bipolar transistor comprises:

a semiconductor substrate having a collector and subcollector region formed therein, wherein said collector is formed between isolation regions that are also present in the substrate;

a SiGe layer formed on said substrate, said SiGe layer including polycrystalline Si regions formed above said isolation regions and a SiGe base region formed above said collector and subcollector regions;

a patterned insulator layer formed on said SiGe base region, said patterned insulator layer having an opening therein;

an emitter formed on said patterned insulator layer and in contact with said SiGe base region through said opening, said emitter having exposed sidewalls;

a conformal passivation layer formed on at least said exposed sidewalls of said emitter; and

silicide regions formed on exposed portions of said SiGe layer and said emitter not covered by said conformal passivation layer.

It is emphasized that the passivation layer is employed in the present invention as a means for preventing bridging between adjacent silicide regions which, if present in the structure, causes silicide shorts.

Brief Description of the Drawings

FIG 1 is a pictorial representation of a prior art SiGe heterojunction bipolar transistor which does not include the passivation layer of the present invention formed on any exposed sidewalls of the emitter.

FIG 2 is a pictorial representation of the inventive SiGe heterojunction bipolar transistor which includes a conformal passivation layer formed on exposed sidewalls of the emitter.

FIGS 3-8 are pictorial representations of the inventive bipolar transistor through various processing steps of the present invention.

Detailed Discussion of the Invention

The present invention which provides a method for improving the SiGe bipolar yield of a SiGe bipolar transistor as well as a SiGe heterojunction bipolar transistor will now be described in more detail by referring to the drawings the accompany the present invention. It is noted that in the accompanying drawings, like and corresponding elements are referred to by like reference numerals. Also, for simplicity, only one bipolar device region is shown in the drawings. Other bipolar device regions as well as digital logic circuitry may be formed adjacent to the bipolar device region depicted in the drawings.

Reference is first made to FIG 2 which represents a cross-sectional view of the inventive SiGe heterojunction bipolar transistor. Specifically, the SiGe heterojunction bipolar transistor comprises semiconductor substrate 50 of a first conductivity type (N or P) having sub-collector region 54 and collector region 56 formed therein. Isolation regions 52 which are also present in the substrate define the outer boundaries of the bipolar device region and serve to isolate the bipolar device region shown in FIG 2 from adjacent device regions.

The SiGe bipolar transistor of FIG 2 also includes SiGe layer 58 formed on substrate 50 as well as isolation regions 52. In accordance with the present invention, the SiGe layer includes polycrystalline Si regions 60 that are formed over isolation regions 52 and SiGe base region 62 which is formed over the collector and subcollector regions. The SiGe base region includes extrinsic base and intrinsic regions; these regions are not separately labeled in the drawings, but are nevertheless meant to be included within region 62. It is noted that the extrinsic and intrinsic base regions of the structure are sometimes referred to as the pedestal portion of a bipolar transistor device.

The bipolar transistor of FIG 2 also comprises a patterned insulator layer 64 which has an opening formed therein and an emitter, i.e., a region of intrinsic polysilicon, 66 formed on said patterned insulator layer and in contact with the SiGe base region through the opening in the patterned insulator layer. The inventive bipolar transistor shown in FIG 2 also includes conformal passivation layer 68 which is present on the exposed sidewalls of emitter 66; conformal passivation layer 68 may also be present on sidewalls of the patterned insulator as well as on a portion of the SiGe base region. Silicide regions 70 are also shown in the inventive bipolar transistor. The silicide regions are formed on the horizontal portion of the emitter as well as exposed portions of SiGe layer 58.

It is noted that the bipolar transistor shown in FIG 2 has improved SiGe bipolar yield because of the presence of the passivation layer which is formed in the structure prior to forming the silicide regions. The passivation layer prevents bridging between adjacent silicide regions which typically occurs in prior art SiGe heterojunction

bipolar transistors. See FIG 1. In the present invention, bipolar yield may be improved as much as 20 to 30%; therefore the present invention provides an improved structure compared with prior art SiGe bipolar transistors which do not contain the passivation layer therein.

The method and various materials that are employed in forming the SiGe heterojunction bipolar transistor shown in FIG 2 will now be described in more detail. Reference is first made to FIG 3 which shows the bipolar device region of an initial structure that is employed in the present invention. The initial structure shown in FIG 3 comprises substrate 50 having sub-collector region 54, collector region 56 and isolation regions 52 formed therein.

The structure shown in FIG 3 is fabricated using conventional processing steps that are well known to those skilled in the art. Moreover, conventional materials are used in fabricating the same. For example, substrate 50 is composed of any semiconducting material including, but not limited to: Si, Ge, SiGe, GaAs, InAs, InP and all other III/V compound semiconductors. Layered substrates comprising the same or different semiconducting material, e.g., Si/Si or Si/SiGe, are also contemplated herein. Of these semiconducting materials, it is preferred that substrate 50 be composed of Si. As mentioned above, the substrate may be a N-type substrate or a P-type substrate depending on the type of device to be subsequently formed.

The structure of FIG 3 is formed by first forming an oxide layer (not shown) on the surface of substrate 50 using a conventional deposition process such as chemical vapor deposition (CVD), plasma-assisted CVD, or sputtering, or alternatively the oxide layer is grown thermally. Sub-collector region 54 is then formed in the substrate using a conventional ion implantation step. After the implantation step, a thick oxide (also not shown), on the order of about 240 nm, is grown on the surface to eliminate implantation damage. Next, the thick oxide as well as the previously mentioned oxide layer are removed utilizing an etching process which has a high selectivity for removing oxide as compared to silicon.

Isolation regions 52 are then formed by either using a conventional local oxidation of silicon (LOCOS) process or by utilizing lithography, etching and trench isolation filling. It is noted that the drawings show the formation of isolation trench regions

which are formed as follows: A patterned masking layer (not shown) is first formed on the surface of substrate 50 exposing portions of the substrate. Isolation trenches are then etched into the exposed portions of the substrate utilizing a conventional dry etching process such as reactive-ion etching (RIE) or plasma-etching. The trenches thus formed may be optionally lined with a conventional liner material, i.e., an oxide, and thereafter CVD or another like deposition process is employed to fill the trenches with silicon oxide or another like trench dielectric material. The trench dielectric material may optionally be densified after deposition and a conventional planarization process such as chemical-mechanical polishing (CMP) may also be optionally employed.

Following the formation of isolation regions in the substrate, collector region 56 is then formed in the bipolar device region (between the two isolation regions shown in FIG 2) utilizing conventional ion implantation and activation annealing processes that are well known to those skilled in the art. The activation annealing process is typically carried out at a temperature of about 950°C or above for a time of about 30 seconds or less.

At this point of the inventive process, the bipolar device region shown in the drawings may be protected by forming a protective material such as Si_3N_4 thereon, and conventional processing steps which are capable of forming adjacent device regions can be performed. After completion of the adjacent device regions and subsequent protection thereof, the inventive process continues. It should be noted that in some embodiments, the adjacent device regions are formed after completely fabricating the bipolar transistor.

The next step of the present invention is shown in FIG 4. In this figure, SiGe layer 58 is formed on substrate 50 as well as isolation regions 52. In accordance with the present invention, the SiGe layer includes polycrystalline Si regions 60 that are formed over isolation regions 52, and SiGe base region 62 which is formed over the collector and subcollector regions.

The SiGe layer is formed epitaxially utilizing any conventional deposition technique including, but not limited to: ultra-high vacuum chemical vapor deposition

(UHVCVD), molecular beam epitaxy (MBE), rapid thermal chemical vapor deposition (RTCVD) and plasma-enhanced chemical vapor deposition (PECVD). The conditions used in forming the SiGe layer (which are conventional and well known to those skilled in the art) vary depending upon the desired technique employed.

Next, and as shown in FIG 5, insulator layer 61 (which will subsequently become patterned insulator 64) is formed on SiGe base layer 62 utilizing a conventional deposition process such as CVD, plasma-assisted CVD, chemical solution deposition and other like deposition processes. The insulator may be a single layer, as is shown in FIG 5, or it may contain multi-insulator layers. The insulator layer is composed of the same or different insulator material which is selected from the group consisting of SiO_2, Si oxynitride and other like insulators.

Emitter window opening 63 is then formed in insulator layer 61 so as to expose a portion of the SiGe base region, See FIG 6. The emitter window opening is formed utilizing lithography and etching. The etching step used is selective in removing the insulator material as compared to the SiGe layer.

Following formation of the emitter window opening, an intrinsic polysilicon layer (which will subsequently become emitter 66) is formed on the patterned insulator and in the emitter window opening by utilizing either a conventional in-situ doping deposition process or deposition followed by ion implantation. The polysilicon and the insulator are then selectively removed so as to form patterned insulator 64 and emitter 66 on SiGe base region 62, See FIG 7. Specifically, lithography and etching are employed in forming the structure shown in FIG 7. It is should be noted that a single etching process may be employed in removing portions of the intrinsic polysilicon layer and insulator layer 61, or separate etching steps may be employed in removing these layers. It is noted that in the structure shown in FIG 7, emitter 66 has exposed sidewalls 69.

Next, as shown in FIG 8, conformal passivation layer 68 is formed on exposed sidewalls 69 of emitter 68 as well as on the vertical sidewalls of patterned insulator 64

and a portion of SiGe base region 62. In accordance with the present invention, the conformal passivation layer is formed utilizing a rapid thermal chemical vapor deposition (RTCVD) process. The passivation layer may be composed of an oxide, an oxynitride, a nitride, or any combination thereof. Of these materials, it is preferred in the present invention that a nitride passivation layer be employed. When a nitride passivation layer is to be formed, the nitride passivation layer is formed by a RTCVD process that is carried out in a nitrogen-containing atmosphere such as NO, N_2O or N_2, at a temperature of about 700°C or higher.

The passivation layer can then be selectively removed using an anisotropic RIE process. This will leave sidewalls protecting the emitter edges and a complete protecting layer over other regions intentionally left passivated via a lithographic process.

Following the passivation of the exposed sidewalls of emitter 66, the structure shown in FIG 8 is subjected to a conventional silicidation process which is capable of forming silicide regions 70 in the structure. Specifically, the silicide regions are formed in portions of SiGe layer 58 that are not protected by the passivation layer. This step of the present invention results in the formation of the structure shown in FIG 2; note in FIG 2, no bridging between adjacent silicide regions, as is the case in FIG 1, is observed.

While this invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the spirit and scope of the present invention. It is therefore intended that the present invention not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.